TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. ITL.0277US

In Re Application Of: **Tinku Acharya**

09/433,337

Serial No.	Filing Date	Examiner	Group Art Unit
~~09/433,337~~	November 2, 1999	Tan V. Mai	~~2124~~ 2184

Invention: **Discrete Filter Having a Tap Selection Circuit**

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **March 20, 2003**

The fee for filing this Appeal Brief is: **$320.00**

☒ A check in the amount of the fee is enclosed.

☐ The Commissioner has already been authorized to charge fees in this application to a Deposit Account. A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **20-1504**
A duplicate copy of this sheet is enclosed.

Signature

Dated: **March 21, 2003**

Fred G. Pruner, Jr., Reg. No. 40,779
Trop, Pruner & Hu, P.C.
8554 Katy Freeway, Suite 100
Houston, Texas 77024
(713) 468-8880 [Phone]
(713) 468-8883 [Fax]

21906
PATENT TRADEMARK OFFICE

CC:

I certify that this document and fee is being deposited on **03/21/2003** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Signature of Person Mailing Correspondence

Debra Cutrona

Typed or Printed Name of Person Mailing Correspondence

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Tinku Acharya	§	Group Art Unit:	2124
Serial No.:	09/432,337	§	Examiner:	Tan V. Mai
Filed:	November 2, 1999	§		
For:	Discrete Filter Having a Tap Selection Circuit	§	Atty. Dkt. No.:	ITL.0277US (P7626)

#10 S. Cutrona 4-22-03

Board of Patent Appeals & Interferences
Commissioner for Patents
Washington, D.C. 20231

RECEIVED
APR 17 2003
Technology Center 2100

APPEAL BRIEF

Dear Sir:

Applicant hereby appeals from the Final Rejection dated February 21, 2003, finally rejecting claims 1-3 and 9-11.

I. REAL PARTY IN INTEREST

The real party in interest is Intel Corporation, the assignee of the present application by virtue of the Assignment recorded at Reel/Frame 010369/0127.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

RECEIVED
2003 MAR 26 PM 2:59
BOARD OF PATENT APPEALS AND INTERFERENCES

Date of Deposit: 3-21-03
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Board of Patent Appeals & Interferences, Commissioner for Patents, Washington, DC 20231.
Debra Cutrona
Debra Cutrona

04/16/2003 AJONES3 00000002 09433337
01 FC:1402 320.00 OP

III. STATUS OF THE CLAIMS

The application was originally filed with claims 1-25. In response to a restriction requirement, claims 1-12 were elected for prosecution, and claims 13-25 were cancelled. Claim 12 was later cancelled; and claims 4-8 have been objected to as being allowable if rewritten in independent form. Claims 1-3 and 9-11 have been finally rejected and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

There are no unentered amendments.

V. SUMMARY OF THE INVENTION

Referring to Fig. 1, an embodiment 5 of a digital filter system in accordance with the invention includes a systolic processing chain 10 that has a selectable number of taps. Due to this architecture, the system 5 may be used to form a wide range of digital filters, as the number of taps may be selected by a programmable tap selection circuit 12 that is coupled to the processing chain 10. As further described below, output terminals 11 of the processing chain 10 may indicate a filtered output value (called y(i)) on each cycle of a clock signal (called CLK_1), a feature that results in 100% throughput for the processing chain 10. Specification, pp. 2-3.

As an example, in some embodiments, the digital filter system 5 may be used to implement a symmetric finite impulse response (FIR) filter. Due to the symmetry (C(n) = C(-n)) of the filter coefficients for this type of filter, Eq. 1 may be simplified, as described by the following equation:

$$y(i) = C(0) \cdot x(i) + \sum_{j=1}^{N} C(j) \cdot (x(i-j) + x(i+j)) \qquad \text{Eq. (2)}$$

In Eq. 2, each "x()" denotes a particular input value, "C()" represents a particular filter coefficient and "y(i)" represents a particular filter output. It may be noted from Eq. 2 that although the number of taps of the filter is 2N+1, the number of filter coefficients (i.e., C(0), C(1), C(2), . . . C(N)) that are used by the filter is equal to N+1. Thus, except for the C(0) filter coefficient (that is associated with one tap of the filter), each C(j) filter coefficient is associated with two taps of the filter due to the symmetry. For example, N equals three for a seven tap filter, and as an example, a particular output value y(10) for the seven tap filter may be described by the following equation:

$$y(10) = C(3) \cdot \{x(9) + x(13)\} + C(2) \cdot \{x(8) + x(12)\} + C(1) \cdot \{x(9) + x(11)\} + C(0) \cdot x(10)$$

Eq. (3)

Thus, except for the C(0) coefficient, each C(j) coefficient is multiplied by a pair of input values (i.e., x(i-j) + x(i+j)). Referring to Fig. 2, in some embodiments, these multiplications may be performed by N+1 processing units 20 (processing units 20_0, 20_1, . . ., 20_k, . . . 20_{n-1}, 20_n, as examples) of the chain 10, each of which exploits the symmetric property of the filter by multiplying a different C(j) coefficient by the appropriate pair of input values. As further described below, the processing units 20 form a systolic architecture, an architecture in which all of the processing units 20 are producing products on each clock cycle of the CLK_1 signal so that the chain 10 produces a different output value on each clock cycle. Specification, p. 3.

More particularly, the processing units 20 are serially coupled together to form a serial chain for forming the output values, a chain in which the processing occurs from the processing unit 20n to the processing unit 20_0. Each processing unit 20 is associated with a different filter coefficient (i.e., each processing unit 20 is associated with two taps of the filter) and generates a corresponding product for each output value. In this manner, each processing unit 20 receives an indication (via accumulation input lines 102) of an ongoing sum from the predecessor processing unit 20 (except for the first processing unit 20n) in the chain 10, updates the ongoing sum with an additional product and furnishes an indication of the ongoing sum (via accumulation output lines 110) to the successor processing unit 20 (except for the last processing unit 20_0) in the chain 10. Specification, pp. 3-4.

Referring to Fig. 3, as an example, a particular processing unit 20k receives three input signals that indicate three respective values: p(k), the broadcast input value (from a broadcast input line 205) that is equivalent to some x value; r (k+1), a delayed input value indicated by the predecessor processing unit 20k+1 (not shown) in the chain 10; and q(k+1), an ongoing sum value indicated by the predecessor processing unit 20k+1 in the chain 10. The processing unit 20k furnishes two output signals (to the successor processing unit 20k-1 (not shown)) that indicate two respective values: r(k) and q(k). Mathematically, r(k) and q(k) may be described by the following equations:

$$r(k) = r(k+1) \qquad \text{Eq. (4)}$$

$$q(k) = q(k+1) + C(x) \cdot \{p(k) + r(k+1)\} \qquad \text{Eq. (5)}$$

Based on the above-described principle of operation, it may be observed that r(k+1)=x(i-j) when p(k)=x(i+j), and thus, for these input values, q(k) = C(j)·[x(i+j)+x(i-j)]. Specification, p. 4.

Referring back to Fig. 2, as an example, in some embodiments, the processing units 20_0, 20_1, . . ., 20_k, . . . 20_{n-1}, 20_n are associated with the C(n), C(n-1), . . . C(k), . . . C(1), C(0) coefficients, respectively, and the processing chain 10 begins with processing unit 20_n and ends with the processing unit 20_0. Thus, as an example, for a particular output value, the processing unit 20n provides the first product (called the C(0) product) by multiplying the x(i) value by C(0). It is noted that for j=0, x(i+j)=x(i-j)=x(i). The product that is provided by the processing unit 20n begins a sum to which all the processing units 20 contribute another product. In this manner, the processing unit 20n-1 receives signals from the processing unit 20 that indicate the C(0)·x(i) product. The processing unit 20n-1 adds the term C(1)·[x(i+1)+x(i-1)], called the C(1) product, to the ongoing sum and furnishes signals to the next processing unit in the chain, etc. Eventually, the processing unit 20_0 adds the last product (the C(N)·[(x+N)+(x-N)] product) to the rolling sum to generate the signal at the output terminals 11. It is noted that when the processing chain 10 receives x(0) to begin the filtering, N+1 clock cycles are consumed to produce the first valid output value. However, thereafter, the processing chain 10 produces an output on every clock cycle, thereby resulting in 100% throughput. Specification, pp. 4-5.

Referring back to Fig. 3, as an example, in some embodiments, the processing unit 20k may include input 22 and output 24 registers that delay the digital signal that indicates each r(k+1) value before communicating the signal to the successor processing unit 20k-1. In this manner, in some embodiments, the input register 22 receives the digital signal that indicates the

r(k) signal (via the input lines 104) on a positive edge (for example) of a processing clock signal (called CLK_1) and communicates the stored digital signal to the output register 24 on the next positive edge (as an example) of the CLK_1 signal. The output register 24 indicates (via the output lines 108) the stored digital signal (i.e., indicates the r(k) value) to the successor input register 22 in the processing chain 10. Specification, p. 5.

The processing unit 20k also includes an adder 32, a multiplier 34 and an adder 36 to generate the q(k) value. In some embodiments, these components are clocked by a clock signal (called CLK_2) that is synchronized to the CLK_1 clock signal and has a frequency that is a multiple of the frequency of the CLK_1 clock signal so that the q(k) signal is generated on each positive edge (for example) of the CLK_1 signal. In this manner, the adder 32 is coupled to receive the digital signal that indicates the r(k+1) value synchronously with the reception of the r(k+1) value by the input register 22. The adder 32 adds this digital signal with a digital signal that indicates the current p(k) value to form an indication of p(k) + r(k+1). The multiplier 34 multiplies the digital output signal from the adder 32 with a digital signal that indicates the associated filter coefficient to produce the digital signal that indicates the $C(k)\cdot[p(k)+r(k+1)]$ signal. The digital signal that indicates the filter coefficient is stored in a coefficient register 30. The coefficient may be changed via data and control lines 16 that are coupled to the register 30. The adder 36 combines the digital output signal from the multiplier 34 with the q(k+1) signal to produce the digital output signal (on the output lines 110) that indicates the q(k) value. Specification, p. 5.

Fig. 4 depicts an example of the integration of the processing chain 10 and the tap selecting circuit 12 to form a selectable tap filter 199 that permits the selection of up to seven taps. In this manner, the filter 199 includes a processing chain of five processing units 20_0, 20_1, 20_2, 20_3 and 20_4. The filter 199 also includes four termination units 100_0, 100_1, 100_2, and 100_3 (of the same design 100) that are associated with the processing units 20_0, 20_1, 20_2, and 20_3, respectively. In this manner, a particular termination unit 100 may be selected (via the appropriate bit in a register 200) to terminate the processing chain at its associated processing unit 20. For example, the termination unit 100_2 may be selected to terminate the processing chain at the processing unit 20_2 and thus, create a five tap processing chain. Similarly, the termination unit 100_1 may be selected to terminate the processing chain at the processing unit 20_1 and thus, create a three tap processing chain. Specification, pp. 5-6.

The selection of a particular termination unit 100 may be accomplished via selection lines 103, each of which extends to a different termination unit 100. In this manner, when a particular selection line 103 is asserted (driven high, for example) the associated termination unit 100 is selected and thus, the number of taps is selected. It is noted that only one selection line 103 is asserted, and the remaining selection lines 103 are deasserted (driven low, for example). The selection lines 103 may indicate respective selection bits of a selection register 200, and the selection bits may be stored in the register 200 via data and control lines 201. Specification, p. 6.

As depicted by the termination unit 100_2, each termination unit 100 may include a multiplexer 124 that selects either the broadcast input lines 205 (when the termination unit 100 is selected) or the output lines 108 (when the termination unit 100 is deselected) of the predecessor

processing unit 20 and couples the selected lines to the input lines 104. The termination unit 100 may also include another multiplexer 122 that selects either the output lines 110 (when the termination unit 100 is selected) of the previous processing unit 20 or the lines 118 (when the termination unit 100 is deselected) indicative of "0" (i.e., a zero sum) and couples the selected lines to the input lines 102. Specification, p. 6.

Referring to Fig. 5, in some embodiments, the processing unit and termination unit may be combined to form a combined unit 300. In this manner, the unit 300 may be replicated to form a processing chain of an arbitrary length. This processing chain may be effectively truncated as needed to suit a particular filtering application, as described above. Specification, p. 6.

VI. ISSUES

A. Can claims 1-3 and 9-11 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 1?

B. Can claim 3 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 3?

C. Can claim 9 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 9?

D. Can claim 10 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 10?

VII. GROUPING OF THE CLAIMS

Claims 1, 2 and 11 can be grouped together; and claims 3, 9 and 10 are each separately patentable for the reasons set forth below. Although claims 1-3 and 9-11 are rejected under the

same ground of rejection, claims 1, 2 and 11 do not stand or fall together with any of claims 3, 9 or 10; and claims 3, 9 and 10 each stand alone. Thus, each of claims 3, 9 and 10 do not stand or fall together with any of the other claims.

VIII. ARGUMENT

All claims should be allowed over the cited references for the reasons set forth below.

A. Can claims 1-3 and 9-11 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 1?

The digital signal processing circuit of independent claim 1 includes a chain of processing units and a tap selection circuit. The chain of processing units receives indications of discrete input values, and each processing unit is associated with one of a group of filter coefficients. The tap selection circuit selects a group of the processing units of the chain to produce an indication of a filtered discrete output value for each discrete input value.

The Examiner rejects independent claim 1 under 35 U.S.C. § 103(a) in view of U.S. Patent No. 6,125,155 (herein called "Lesthievent"). Lesthievent generally teaches a digital filtering method and a filter that implements the method. More particularly, Lesthievent depicts several filter architectures, such as the filter architecture that is depicted in Fig. 4 of Lesthievent. This architecture includes Q physical stages and an array of switches S(0), S(1),..., S(Q-1). The switches are activated at an output frequency rate Fs to multiply input data with filter coefficients. *See generally,* Lesthievent, 2:44-65. However, Lesthievent neither teaches nor suggests a tap selection circuit. In other words, there is no circuitry in Lesthievent to select the taps of any of the disclosed filter architectures.

The Examiner acknowledges that Lesthievent does not teach a tap selection circuit. In this regard, the Examiner states in the Final Office Action, "it is noted that Lesthievent et al do not show the claimed 'tap selection circuit'." Final Office Action, 2. However, the Examiner goes on to state in the Final Office Action that Lesthievent teaches a circuit to allegedly perform the function that is recited in lines 4 and 5 of claim 1. Thus, the Examiner concludes a case of obviousness for claim 1 because, "the switches s(i) are capable of providing the equivalent function, i.e., select a group of processing units having multipliers g(i)." *Id.*, 2.

To establish a *prima facie* case of obviousness, there must be a suggestion or motivation to modify a reference to derive a missing claim limitation. M.P.E.P. § 2143. Furthermore, the Examiner must point to specific language in the prior art establishing the alleged suggestion or motivation to modify a reference to derive the missing claim limitations. *Ex parte Gambogi*, 62 USPQ2d 1209, 1212 (Bd. Pat. App. & Int. 2001); *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2143. Thus, the Examiner has improperly concluded a case of obviousness for claim 1 without providing support for the alleged suggestion or motivation.

In summary, Lesthievent fails to show a tap selection circuit, and the Examiner fails to show any support for the alleged suggestion or motivation to modify Lesthievent to derive the missing tap selection circuit. Therefore, for at least these reasons, a *prima facie* case of obviousness has not been established for independent claim 1.

Claims 2, 3 and 9-11 are patentable for at least the reason that these claims depend from an allowable claim.

Thus, for at least the reasons set forth above, the § 103(a) rejections of claims 1-3 and 9-11 are improper and should be reversed.

B. Can claim 3 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 3?

Claim 3 depends from independent claim 1 and recites that the tap selection circuit selects a number of taps of the processing circuit.

The Examiner rejects dependent claim 3 under 35 U.S.C. § 103(a) in view of Lesthievent. Claim 3 is patentable for at least the reason that claim 3 depends from an allowable claim, as set forth above in the discussion of Issue A. Claim 3 is patentable for the additional, independent reason set forth below.

As noted above, the Examiner admits that Lesthievent does not disclose a tap selection circuit. Thus, Lesthievent cannot teach a circuit to select a number of taps. Furthermore, the Examiner fails to show any support for the alleged suggestion or motivation to modify Lesthievent so that one of its circuits selects a number of taps. Such a suggestion or motivation is required to establish a *prima facie* case of obviousness. Therefore, for at least these reasons, the Examiner fails to establish a *prima facie* case of obviousness for dependent claim 3.

The Examiner states, "the switch s(i) are capable of selecting number of 'processing units having multipliers g(i)'." First Office Action, 3. However, the mere fact that references can be combined or modified is insufficient by itself to establish a *prima facie* case of obviousness. *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01.

Thus, for at least these additional, independent reasons, the § 103(a) rejection of claim 3 is improper and should be reversed.

C. Can claim 9 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 9?

The processing circuit of claim 9 depends from independent claim 1 and recites that the tap selection circuit includes a register that stores bits indicative of the processing units in the group.

The Examiner rejects claim 9 under 35 U.S.C. § 103(a) as being unpatentable in view of Lesthievent. Claim 9 is patentable for at least the reason that claim 9 depends from an allowable claim, for the reasons set forth above in connection with the discussion of Issue A. Claim 9 is patentable for the additional, independent reason set forth below.

In the rejection of claim 9, the Examiner states that, "the detail features are old and well known in the art." First Office Action, 4. However, even assuming, *arguendo,* that registers may be well known in the art, there must be a suggestion or motivation to modify Lesthievent so that Lesthievent includes such a register. The Examiner provides absolutely no support for the alleged suggestion or motivation to modify one of its disclosed filter architectures so that the architecture includes such a register. Therefore, for at least this additional, independent reason, the Examiner fails to establish a *prima facie* case of obviousness for claim 9.

Thus, the § 103(a) rejection of claim 9 is improper and should be reversed.

D. Can claim 10 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for claim 10?

Claim 10 depends from independent claim 1 and recites that each processing unit includes a register that stores an indication of an associated filter coefficient.

The Examiner rejects claim 10 under 35 U.S.C. § 103(a) as being unpatentable in view of Lesthievent. Claim 10 is patentable for at least the reason that claim 10 depends from independent claim 1 for the reasons set forth above in the discussion of Issue A. However, claim 10 is patentable for the additional, independent reasons set forth below.

The Examiner contends that a register that stores indication of an associated filter coefficient is allegedly old and well known in the art. First Office Action, 4. However, even assuming, *arguendo*, that the Examiner's statement is correct, the Examiner provides no support for the alleged suggestion or motivation to modify Lesthievent to include this feature. Therefore, for at least this additional, independent reason, the Examiner fails to establish a *prima facie* case of obviousness for dependent claim 10.

Thus, the § 103(a) rejection of claim 10 is improper and should be reversed.

IX. CONCLUSION

Applicant requests that each of the final rejections be reversed and that the claims subject to this appeal be allowed to issue.

Respectfully submitted,

Date: 3/24/03

Fred G. Pruner, Jr., Reg. No. 40,779
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Suite 100
Houston, Texas 77024-1805
(713) 468-8880 [Phone]
(713) 468-8883 [Facsimile]

APPENDIX OF CLAIMS

The claims on appeal are:

1. A digital signal processing circuit comprising:

a chain of processing units to receive indications of discrete input values, each processing unit being associated with one of a group of filter coefficients; and

a tap selection circuit to select a group of the processing units of the chain to produce an indication of a filtered discrete output value for each discrete input value.

2. The processing circuit of claim 1, wherein the chain of processing units comprises a systolic chain.

3. The processing circuit of claim 1, wherein the tap selection circuit selects a number of taps of the processing circuit.

9. The processing circuit of claim 1, wherein the tap selection circuit comprises:

a register storing bits indicative of the processing units in the group.

10. The processing circuit of claim 1, wherein each processing unit comprises:

a register storing the indication of the associated filter coefficient.

11. The processing circuit of claim 1, wherein the processing units and tap selection circuit comprise at least part of a finite impulse response filter.